

JCS(01)8

09/989667 PTO

**ISSUE CLASSIFICATION**

PATENT NUMBER  
1,234,567

**U.S. UTILITY Patent Application**

 <b>O.I.P.E.</b> SCANNED  Q.A. 	<b>PATENT DATE</b>
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APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/989667		710	305	2181	Aure

Francis Joseph

System-On-Chip architecture that utilizes FeRAM and re-configurable hardware

PTO-2040  
12/99

## **ISSUING CLASSIFICATION**

Continued on Issue Slip Inside File Jacket

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.  _____  _____				<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____  _____  _____				<b>ISSUE FEE</b>	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.				Amount Due	Date Paid
				<b>ISSUE BATCH NUMBER</b>	
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